Semester: 5th			
Paper code: AIDS307/AIML307	**L**	**T/P**	**Credits**
Subject: Computer Organization & Architecture	**3**	**0**	**3**

Marking Scheme:

1. Teachers Continuous Evaluation: As per university examination norms from time to time
2. End Term Theory Examination: As per university examination norms from time to time

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks: As per university norms

1. There should be 9 questions in the end term examination question paper.
2. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions.
3. Apart from Question No. 1, the rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, students may be asked to attempt only 1 question from each unit.
4. The questions are to be framed keeping in view the learning outcomes of course/paper. The standard/ level of the questions to be asked should be at the level of the prescribed textbooks.
5. The requirement of (scientific) calculators/ log-tables/ data-tables may be specified if required.

Course Objectives:

1.	To understand the basic concepts of computer operation.
2.	To analyze different memory hierarchies along with their mapping.
3.	To apply and analyze different pipelining and parallelism.
4.	To implement various signed and unsigned arithmetic operations with digital hardware.

Course Outcomes:

CO1	Interpreting the basic concepts of register transfer language and computer operations.
CO2	Apply and analyze various instruction formats for CPU/GPU together with a variety of addressing modes.
CO3	Analyze different types of Parallel Computer Models.
CO4	Implementing arithmetic operations with digital hardware.

Course Outcomes (CO) to Programme Outcomes (PO) Mapping

(Scale 1: Low, 2: Medium, 3: High)

CO/ PO	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO1	1	1	1	1		1						2
CO2	2	1	1	1							1	3
CO3	3	2	3	2	1	1	1				1	3
CO4	1	1	1	1								2

Course Overview:

This course enables the students to understand the principles of computer organization and the basic architectural concepts. It begins with basic organization, design, and programming of a simple digital computer and introduces simple register transfer language to specify various computer operations. Topics include computer arithmetic, instruction set design,

microprogrammed control unit, pipelining and vector processing, memory organization and I/O systems, and multiprocessors.

Unit I **[8]**

Register Transfer Language: Register transfer language, bus and memory transfer, bus architecture using multiplexer and tri-state buffer, micro-operation: arithmetic, logical, shift micro-operation with hardware implementation, arithmetic logic shift unit.

Computer Organization and Design: Instruction codes, general computer registers with common bus system, computer instructions: memory reference, register reference, input-output instructions, timing and control, instruction cycle, input-output configuration, and interrupt cycle. Levels of programming languages: Machine language, Assembly language, High level language.

Unit II **[8]**

Central processing Unit: Introduction, general register organization, stack organization, instruction format, addressing modes. Overview of GPU, CPU vs GPU computing difference.

Memory Hierarchy: Introduction, basics of cache, measuring and improving of cache performance, cache memory: associative mapping, direct mapping, set-associative mapping, cache writing and initialization, virtual memory, common framework for memory hierarchies. Case study of PIV and AMD opteron memory hierarchies.

Unit III **[8]**

Parallel Computer Models: The state of computing, classification of parallel computers, multiprocessors and multicomputers, multivector and SIMD computers. Program and Network Properties: conditions of parallelism, data and resource dependences, hardware and software parallelism, program partitioning and scheduling, grain size and latency, program flow mechanisms, control flow versus data flow, data flow Architecture, demand driven mechanisms, comparisons of flow mechanisms.

Unit IV **[8]**

Pipelining: Introduction to Flynn‘s classification, arithmetic pipeline, instruction pipeline, pipeline conflict and hazards, RISC pipeline, vector processing.

Arithmetic for Computers: Unsigned, signed 1‘s, 2‘s compliment notations, addition, subtraction, multiplication and division (hardware implementation), CPU performance and its factors, evaluating performance of CPU.

Textbooks:

1. M. Morris, Mano, “Computer System Architecture”, PHI 3rd Edition 2007.
2. Kai Hwang, “Advanced computer architecture”; TMH. 2000
3. D. A. Patterson and J. L. Hennessey, “Computer organization and design”, Morgan Kaufmann, 2nd Ed. 2002

Reference Books:

1. W. Stallings, “Computer organization and Architecture”, PHI, 7th ed, 2005.

2. Harvey G.Cragon,"Memory System and Pipelined processors"; Narosa Publication. 1998
3. V.Rajaranam & C.S.R.Murthy, "Parallel computer"; PHI. 2002
4. R.K.Ghose, Rajan Moona & Phalguni Gupta, "Foundation of Parallel Processing", Narosa Publications, 2003.